REMARKS

Claims 1 to 20 are pending. The claims have been amended for clarity.

The Office Action cites Arndt et al. (US 2005/0018669 A1) and Franke et al. (US 6542513) and alleges that the pending claims are obvious in light of the combination of Arndt et al. and Franke et al. The Office Action, as understood, relies upon Francke et al. only in relation to claims 6, 7, 13 and 14.

Independent Claims 1 and 11

As previously pointed out, the Applicant submit that the rejection of the claims is incorrect at least because:

- claim 1 recites " a full-duplex packetized interconnect directly connecting a CPU of the first compute node to a first network interface connected to the inter-node communication network"; and
- claim 11 recites "a dedicated full-duplex packetized interconnect directly coupling the CPU to the network interface".

As explained in detail below, the cited references, as understood, fail to disclose or suggest these features in the contexts of claims 1 and 11 respectively.

The Office Action quotes text from paragraphs [0030], [0035], [0042], [0043] and [0044] of Arndt as disclosing these claimed features. The Office Action does not indicate what element described by Arndt is being equated to the claimed full-duplex packetized interconnect. As far as Arndt is understood, the Office Action is incorrect in this regard.

Paragraphs [0030] and [0035] of Arndt do not disclose, within a compute node, a CPU directly connected to a first network interface by a full-duplex packetized interconnect, as claimed in claims 1 and 11.

Arndt paragraph [0042] discloses that 'User clients can bypass the operating system kernel process and directly access network communication hardware, such as host channel adapters ..." This section is referring to the software architecture of the Arndt system and does not

disclose a CPU directly connected to a first network interface. Note that all of the cited paragraphs are describing the SAN (100) shown in Fig. 1 of Arndt. That Figure explicitly shows CPUs 126, 128, 130, 136 138 and 140. None of those CPUs is illustrated as being directly connected to any network interface (by a full-duplex packetized interconnect or otherwise). The Examiner's attention is also directed to paragraph [0039] of Arndt which states that 'the host channel adapters and SAN 100 ... provide ... zero processor-copy data transfers ...' (see par [0039], ln. 11). This suggests that the Arndt system has no need for a direct connection between a CPU and a network interface.

The portion of Arndt quoted in the Office Action also states that 'I/O adapter nodes' can communicate with processor nodes. The Applicant point out that the processor nodes cannot be equated to the claimed CPUs. Arndt Fig 1. shows processor nodes (102, 104) which are separate from and contain CPUs 126, 128, 130, 136, 138 and 140. It can be seen that the CPUs are not directly connected to any interfaces.

The Office Action also alleges (on page 11) that this feature is disclosed by Arndt at the following locations: [0034] ln. 1-5; [0037] ln. 1-15; and [0038] ln. 1-3. This too is incorrect, as Arndt is understood.

- The quoted section of [0034] describes a switch.
- [0037] describes host channel adapters (HCAs) in processor nodes (102 and 104). Arndt, as understood, does not disclose a direct connection between the CPUs of a processor node (102, 104) and the HCAs of the processor node. This can be seen in Fig. 1. Note that bus systems (132) and (144) do not connect to the corresponding HCAs.
- The cited portion of [0038] discloses that host channel adapters are connected to switches.

In the absence of a disclosure in the cited references of "a full-duplex packetized interconnect directly connecting a CPU of the first compute node to a first network interface of the first compute node" as claimed in claim 1; or "a dedicated full-duplex packetized interconnect directly

coupling the CPU to the first network interface" as claimed in claim 11, the Applicant submit that claims 1 and 11 are in condition for allowance.

Therefore, claims 1 and 11 are submitted to be patentable over the cited references.

Since the Examiner has expressed the view that these features are disclosed in Arndt whereas the Applicant, having reviewed Arndt, cannot see that Arndt discloses these features, the Applicant respectfully requests that the Examiner contact the undersigned by telephone when the Examiner has reached this case for further consideration to arrange an interview in which to discuss the basis for the rejection of claims 1 and 11.

Dependent Claims

The dependent claims are submitted to further distinguish the cited references. Reasons for this are set out in the Response filed on 15 May 2008. Those reasons are submitted to remain valid notwithstanding the position taken in the Office Action.

Claims 2 and 12

Claims 2 and 12 respectively recite that "the first network interface and the CPU are the only devices configured to place data on the packetized interconnect" and "the dedicated packetized full-duplex interconnect is not shared by any devices other than the CPU and the first network interface". The Office Action indicates at d. on page 4 that this feature is disclosed by Arndt at [0066] to [0070]. This section of Arndt describes the use of queue pairs by user-mode software processes to transfer data. A local queue pair is associated with one and only one remote queue pair.

This section, as understood, says nothing regarding the hardware (408) on which data is actually transferred. In particular, this section, as understood, does not disclose a packetized interconnect shared only by the first network interface and the CPU, as claimed.

Also, the Arndt queue pairs queue pairs are apparently located in the host channel adapter (HCA) see [0049] at ln. 4. It is not understood on what basis the Examiner has concluded that

the provision of queue pairs in a host channel adapter constitutes disclosure of a packetized interconnect shared only by the first network interface and the CPU, as claimed.

Also, this section describes the use of zero processor-copy data transfer. This points away from the need for a dedicated connection between a CPU and network interface.

The Office Action also indicates that the features of claims 2 and 12 are disclosed at [0047], ln. 5-15; [0048], ln. 1-13; and [0053] ln. 1-16.

The Applicant submits that this is incorrect. The cited portions of Arndt , as understood, describe higher-level software constructs and do not disclose the features that they are cited for.

Therefore, claims 2 and 12 are submitted to further distinguish the cited references. Again the Examiner is invited to contact the undersigned to discuss this when the Examiner reaches this Amendment for consideration.

Claims 5 and 19

Claim 5 recites "at the network interface, determining a size of the data and, based upon the size of the data, selecting among two or more protocols for transmitting the data". Claim 19 recites "the network interface comprises a facility configured to determine a size of data to be transmitted to another compute node and, based upon the size, to select among two or more protocols...".

The Office Action indicates that these features are disclosed in Arndt at [0101] to [0109] and [0059]. The Applicant has carefully reviewed these sections of Arndt and can find no mention of selecting among different protocols based upon the size of data, as alleged by the Examiner. These sections do describe that the transport layer may provide four types of transport services. However, there appears to be no suggestion of selection among these services on the basis of data size.

The Office Action also alleges that the features of claims 5 and 19 are disclosed in [0058], ln. 1-7; [0060] ln. 1-11; and [0067] ln. 1-6. The Applicant submits that this is incorrect.

- [0058] discloses work queue elements;
- [0060] describes work requests;
- [0067] describes that a queue pair is set to provide a selected type of transport service when the queue pair is created. There is no suggestion that the selection of an available type of transport service is performed based on data size, as claimed. It is not clear how this could be since one would not typically know what data is to be transmitted at the time a queue pair is created.

Therefore, claims 5 and 19 are submitted to further distinguish the cited references. Again the Examiner is invited to contact the undersigned to discuss this when the Examiner reaches this Amendment for consideration.

Claim 17

Claim 17 recites " `A compute node ... comprising a plurality of CPUs each connected to the interface by a separate dedicated full-duplex packetized interconnect.`" Applicant submit that this feature is not disclosed by either of Arndt et al. or Franke et al., as understood. Arndt et al., as understood discloses that all processors are interconnected by a shared bus system (134, 144). Franke et al., as understood, does not remedy this defect.

The Office Action indicates that this feature is disclosed by Arndt at [0029], ln. 1-13; [0030] ln. 1-5 and [0033], ln. 1-12 (see bottom of page 9) . This is submitted to be incorrect. The applicant has reviewed these sections carefully and can find no suggestion of "`a plurality of CPUs each connected to the interface by a separate dedicated full-duplex packetized interconnect`" as claimed. Therefore claim 17 is submitted to be patentable over the cited combination of Arndt et al. and Franke et al.

Claim 18

Claim 18 recites "`the CPU is connected to each of a plurality of network interfaces by a corresponding one of a plurality of dedicated full-duplex packetized interconnects`". As discussed above,

Arndt et al. does not disclose a CPU connected to even one network interface by a dedicated full-duplex packetized interconnect. Arndt et a., as understood, fails to disclose the feature of claim 18. Franke et al., as understood, also fails to describe or suggest the feature of claim 18.

In the section beginning at the bottom of page 14, the Office Action alleges that this feature is disclosed by Arndt. However, the ensuing discussion does not appear to relate to this feature.

In the absence of a disclosure in the cited references of a CPU "`connected to each of a plurality of network interfaces by a corresponding one of a plurality of dedicated full-duplex packetized interconnects`" claim 18 is submitted to be patentable over the cited combination of Arndt et al. and Franke et al.

Conclusion

The Applicant submit that the comments above address all issues raised in the Office Action and that claims 1 to 20 are in condition for allowance. Reconsideration and allowance of this application is respectfully requested.

Respectfully submitted,

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